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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EJC

Office Action Summary	Application No.	Applicant(s)	
	10/771,023	LUNG, HSIANG LAN	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/23/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/3/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Updated Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Amendment after Non-Final Rejection and the Information Disclosure Statement, both filed on November 23, 2005.

2. Claims 1-29 are pending in the case. Claims 1, 16, and 17 are independent claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 14, 17, 18-23, and 28 are rejected are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of $SiNO_2$/SiN/High *k* Dielectrics, Al_2O_3 for SONOS Type Flash Memory", Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163).

5. **Regarding claims 1 and 17,** the applicant has amended these claims to include the phrase "while limiting program and erase cycling" to further explain how the memory cells are programmed and erased. Sakui further teaches that "only one program" and "only one erase" operations can be performed (column 24, lines 1-11). This ~~was~~ previously stated rejection ~~was necessitated by the amendment to the claims.~~ as stated in the 8/23/05 office action is maintained.

2/16/06

6. **With respect to claims 2-5 and 18-20**, Sakui teaches all the claimed elements but doesn't mention anything about the barrier height and thickness of the tunneling dielectric. Lee teaches, in sections 1 and 2, that the new SONOS device has a tunneling dielectric composed of silicon dioxide, having a thickness greater than 30 Angstroms. This is a barrier height and thickness that is sufficient to prevent direct tunneling. Also, in section 3 and Figure 7, a specific example is taught where the tunneling dielectric is 40 Angstroms, which falls inside the range of 30-70 Angstroms. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use these tunneling dielectric thicknesses to prevent direct tunneling in order to reduce the instances of charge loss, as mentioned above.

7. **With respect to claims 6 and 21**, Sakui teaches all the claimed elements but doesn't mention specific positive voltage values. Lee teaches, in section 3, that the positive voltage applied to program and erase a SONOS device can increase up to 18 volts. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to apply a positive voltage of 15 volts or greater because a larger difference in the positive voltage and ground allows for more effective Fowler-Nordheim tunneling.

8. **With respect to claims 7 and 22**, Sakui further teaches, in column 1, lines 50-60, an equation that describes Fowler-Nordheim tunneling. Sakui goes on to say that tunneling begins when the electric field is 10 volts over 10 nm, or 5 volts over 5 nm. As mentioned in the above paragraph, Lee teaches the application of a high positive voltage of 15 volts or higher. In applying the equation taught by Sakui, the electric field resulting from the teaching of Lee will be 15 volts over 5 nm, or greater. It would have

been obvious to one of ordinary skill in the art, at the time of the invention, to apply the well-known equation of Sakui to the positive voltage taught by Lee in order to get an electric field of 15 volts over 5 nm, or greater, in order to achieve more effective Fowler-Nordheim tunneling.

9. **With respect to claim 8**, Sakui teaches in column 1, lines 12-16, that the array of memory cells is configured as a read only memory.

10. **With respect to claims 9 and 23**, Sakui further teaches in Figure 20, and Column 12, lines 50-55, that the cells in the array have a negative threshold voltage prior to programming. Because F-N tunneling requires a high positive voltage applied to the gate, and a low voltage applied to the channels, the threshold voltage will be negative.

11. With respect to claims 14 and 28, Sakui teaches all the claimed elements but doesn't mention a charge trapping structure comprised of silicon nitride. Lee teaches, in section 2 and Figure 1, a charge trapping structure comprised of silicon nitride. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have a charge trapping structure comprised of silicon nitride due to its good charge trapping properties and its relation to the hole current through a tunnel oxide and the electron current through a blocking layer.

12. Claims 15 and 29 rejected under 35 U.S.C. 103(a) as being unpatentable the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of $SiNO_2$/SiN/High *k* Dielectrics, Al_2O_3 for SONOS Type Flash Memory", Extended Abstracts of the 2002

International Conference on Solid State Device and Materials, Nagoya (2002), 162-163), and further in view of the non-patent literature (Liao et al., "Process Techniques and Electrical Characterization for High-k (HfO_xN_y) Gate Dielectric in MOS Devices", Proceedings, 7th International Conference on Solid-State and Integrated Circuits Technology, Volume 1, Oct. 2004, 372–377).

13. **With respect to claim 15**, Sakui and Lee teach all the claimed elements except for a charge trapping structure comprising a metal oxide material. Liao teaches, in the abstract and section 1, a metal oxide semiconductor device having a metal oxide (HfO_x) as a charge trapping structure. It also teaches a combination with this metal oxide with nitride (HfO_xN_y) in order to reduce strain and increase reliability. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use a metal oxide as a charge trapping structure instead of silicon nitride, especially a compound comprised of both substances, as they are both widely used as charge trapping materials.

14. **Regarding claim 29,** the applicant has also amended this claim to express that the charge trapping structure comprises "a metal oxide." Sakui and Lee teach all the claimed elements but fail to explicitly teach a charge trapping structure comprising a metal oxide. Liao teaches, in the abstract and section 1, a metal oxide semiconductor device having a metal oxide (HfO_x) as a charge trapping structure. Liao also teaches a combination with this metal oxide with nitride (HfO_xN_y) in order to reduce strain and increase reliability. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use a metal oxide as a charge trapping structure instead of

silicon nitride, especially a compound comprised of both substances, as metal oxides are widely used in the art as charge trapping materials. This new rejection was necessitated by the amendment to the claim.

15. Claims 10, 16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of $SiNO_2$/SiN/High *k* Dielectrics, Al_2O_3 for SONOS Type Flash Memory", Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163), and further in view of the US Patent to Eitan (5,768,192).

16. **With respect to claims 10, 16 and 24**, Sakui and Lee teach all the claimed elements except the memory array is configured for one-time programming. Eitan teaches, in column 1, lines 7-10, and column 2, lines 41-46, the use of an array of memory cells configured for one-time programming, namely in a PROM, which is a one-time programmable device. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to configure the memory array for one-time programming as it reduces the production cost and allows for better endurance characteristics.

17. Claims 11-13, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakui et al. (6,307,807) in view of the non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of $SiNO_2$/SiN/High *k* Dielectrics, Al_2O_3 for SONOS Type Flash Memory", Extended

Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163), and further in view of the US Patent to Johnson et al. (5,343,437).

18. **With respect to claims 11 and 25**, Sakui and Lee teach all the claimed elements, as mentioned above, except for a static random access memory device and logic which accesses data stored in the array of memory cells. Johnson teaches, in column 2, lines 8-10, an integrated circuit containing both nonvolatile memory and a static random access memory array, including logic that accesses data from both memories. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to connect a nonvolatile memory array to a volatile memory array for the purpose of preserving the advantages of the nonvolatile memory while enjoying the higher performance advantages of high speed volatile memories, such as SRAMS (see column 2, lines 54-57).

19. **With respect to claims 12-13 and 26-27**, Sakui and Lee teach all the claimed element, as mentioned above, except for the use of a processor in an SRAM that executes instructions. Johnson teaches, in column 6, lines 61-68, and column 7, lines 1-5, the use of a processor that executes instructions, including instructions for access to data stored in the nonvolatile and volatile memories and logic that comprises instructions executed by the processor. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use a processor in this manner in order to provide flexibility to update data or instructions as necessary (see column 7, lines 2-3).

Response to Arguments

20. Applicant's arguments filed on November 23, 2005 have been fully considered but they are not persuasive for the reasons listed below.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the applicant asserts that the motivation for combining the teachings of Sakui et al. and Lee et al. is flawed because it would be replacing a floating gate memory cell with good data retention with a SONOS memory cell with bad data retention. The applicant also asserts that Sakui et al. specifically teaches away from the use of a SONOS cell by citing the teachings of Lancaster et al.

The examiner agrees with the applicant that the NAND style flash memory exhibits good data retention characteristics, while conventional SONOS memory cells exhibit poor data retention characteristics, as mentioned in the present application paragraph 0005. The examiner also agrees that Sakui et al. does, in fact, teach away from the conventional SONOS cell disclosed by Lancaster et al. It is made of record that, while conventional SONOS cells do exhibit poor data retention characteristics, this is not the reason why Sakui et al. teaches away from the cell. Sakui et al. merely

states, as argued by the applicant, that "the present invention can provide a remarkable effect different from those of...the memory cell in [Lancaster et al.]...". However, the motivation to combine the teachings of Sakui et al. with the teachings of Lee et al. is upheld because the cell taught by Lee et al. is not a conventional SONOS cell of the type taught by the applicant and Lancaster et al. Lee et al. admits that conventional NAND-type SONOS has considerable charge loss (poor data retention) due to the fact that the tunnel oxide is so thin. This is precisely the reason why Lee et al. has modified the conventional SONOS cell. In the second paragraph of the introduction, Lee et al. teaches that this new SONOS cell structure achieves long data retention and realizes low voltage programming. Because of these properties, this new SONOS cell taught by Lee et al. could indeed be substituted for the cells of Sakui et al. because the problem of poor data retention as been rectified. Also, the examiner argues that the cell of Lee et al. would be more desirable for the system of Sakui et al. due to the power consumption and scalability advantages of the cell of Lee et al. over the cell of Sakui et al.

The applicant also asserts that column 1, lines 12-16 of Sakui et al. does not suggest a read-only memory. Sakui et al. is describing certain EEPROM prior art as the background of his invention. These teachings of Sakui et al. address the content of claim 8 of the present application because EEPROM's are well-known types of read-only memories.

The applicant also asserts that the teaching of a negative threshold voltage by Sakui et al. for the floating gate cell would seem irrelevant if the cell were replaced by

the cell taught by Lee et al. In the introduction of Lee et al., it is mentioned that the new cell realizes low voltage programming. It is obvious that if the new cell of Lee et al. was inserted in the system of Sakui et al., not all the exact teachings applicable to the old cell would apply to the new cell. Because the cell of Lee et al. does indeed realize low voltage programming (and negative voltage is low voltage), the cell of Lee et al. is similar to the cell of Sakui et al. in this respect, and would be a better choice due to the other advantages it holds as mentioned previously in this action.

The applicant goes on to assert that Sakui et al. and Lee et al. combined do not suggest configuring a memory for one-time programming, or otherwise limiting erase cycles, to avoid damage to the tunnel dielectric in the memory cell as described herein.

In response to applicant's argument that the references fail to show certain features of applicant's invention, the examiner has explained the valid combination of Sakui et al. and Lee et al. in the previous paragraphs of this action. The examiner further uses Eitan with this combination to corroborate the fact that a cell, common to the present field of endeavor of ROM's and cells having ONO structures, that is configured for one-time programming is well-known in the art. As a result, some teachings specific to the structures of Eitan (i.e., that the programming is accomplished by using hot electron channel injection rather than E-field assisted tunneling), would obviously not apply to the teachings of Sakui et al. and Lee et al. It is also noted that some of the features upon which applicant relies in this and previous arguments (i.e., that the reason for one-time programming, or limiting erase cycles, is to avoid damage to the tunnel dielectric memory cell) are not recited in the rejected claim(s). Although

the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
1/24/06

2/6/06

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